REMARKS/ARGUMENTS

Claims 1-6, 15-26, and 31-38 are currently pending in the present patent application.

In Section 2 of the Office Action mailed September 26, 2007, new Examiner Movva rejects claims 1-6, 15-26, and 31-38 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0025630 A1 to Tanimoto et al. ("Tanimoto") in view of U.S. Patent No. 5,923,063 to Liu et al. ("Liu"). The Examiner alternately rejects claims 1 and 6 under Section 103(a) as being unpatentable over Tanimoto in view of U.S. Patent Application Publication No. 2001/0038132 A1 to Ahn et al. ("Ahn").

Prosecution of the present application has been particularly frustrating for the undersigned up to this point in time, and the undersigned looks forward to working with new Examiner Movva in reaching agreement on allowable subject matter in the present application. The undersigned requests that the Examiner contact him at (425) 455-5575 to arrange for a telephone interview to further prosecution of this application if, upon consideration of this amendment, the Examiner does not consider all claims in condition for allowance. Should the Examiner have any questions the undersigned requests the Examiner to contact him at this same number to arrange for a telephone interview to discuss the issues.

First, newly cited references Tanimoto, Liu, and Ahn will be discussed before turning to the specific language of the claims. Tanimoto is a representative example of the prior art. With regard to the Examiner's comments about Tanimoto, the Examiner points to Figures 4a-5d and concludes that dielectric layer 107 completely fills a space between adjacent memory cells coupled to the same word line. See Office Action, page 3, lines 9-10. As shown in Figure 4C, it appears in Tanimoto that the space W between adjacent memory cells belonging to the same word line is filled by dielectric layer 107 and by conductive layer 109 (at fixed potential), which stops possible capacitive coupling between floating gates. The dielectric layer 107 accordingly does not completely fill the space between adjacent memory cells coupled to the same word

line. Moreover, with the scaling of devices, the thickness of layer 107 becomes comparable with the spacing W between floating gates 105 and it is no longer possible to insert a conductive layer 109 to screen the floating gates. As a consequence capacitive coupling between neighboring floating gates 105 influences the stored charge, and it is presently considered a primary limitation to the scaling of FLASH memories. The dielectric 107 is multilayer including Silicon Nitride (see col. 3, paragraph 49, 4th sentence from the bottom), which has a high dielectric constant. The use of this material is motivated by the need to have a high capacitive coupling between the top of the floating gate 105 and the control gate (conductive layer 109).

The Ahn patent simply discloses the use of porous silicon oxycarbide as a low-k porous silicon oxycarbide insulator 140. The dielectric 140 is used to insulate active areas and polysilicon from a first metal level. The technology does not apply to FLASH memories, and in fact such a porous dielectric could not be applied to FLASH technology due to its poor contamination resistance. Furthermore, note that in Figure 3 of Ahn the dielectric 140 is deposited above the gate 125 and gate insulator 120 to insulate them from metal layer 300. The dielectric 140 is not formed below the gate structure and accordingly is ineffective for insulating floating gates along the word line direction.

The Liu patent discloses insulating floating gates with a low-k fluorine-doped SiO2 layer (see col. 6, line 32). The deposition of this low-k layer is made inside the trench 42 (Figure 8a) which separates the cells along the bit-line direction, and therefore in the direction orthogonal to the world line. In Liu, the deposition takes place in the trenches 42, which are opened after deposition and definition of the control gate 34, and therefore the low-k dielectric, according to the disclosure by Liu, cannot be deposited between the floating gates 26 and below the control gates 34.

Turning now to the claims, please note that independent claims 1, 16, 21, 24, and 31 have been amended to further clarify the recited subject matter and further evidence the manifest distinctions between these claims and all prior art references of record in the present application. These claims in no way necessitate a new search by the Examiner.

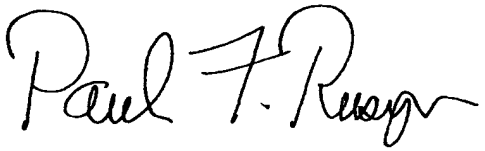
Amended claim 1 recites a non-volatile memory cell integrated on a semiconductor substrate and including a floating gate transistor including a source region and a drain region. The gate region projects from the substrate and is between the source and drain regions. The gate region has a predetermined length and width and includes a first floating gate region and a control gate region. The floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric region with a low dielectric constant value that is formed under the control gate region and between adjacent floating gate regions.

Independent claims 16, 21, 24, and 31 are allowable for reasons similar to the reasons claim 1 is allowable as discussed above, and thus these claims will not be discussed separately herein. Furthermore, all claims which depend from claims 16, 21, 24, and 31 are allowable for at least the same reasons as the associate independent claim and due to the additional limitations added by the dependent claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. If the need for any fee in addition to any fee paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



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